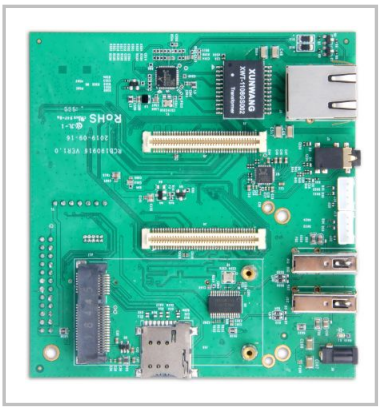
DB-N8MM Hardware Usermanul

V1.0

----------Product modality----------

SoM-N*MM

Gum Stick



CBD96-N8MM

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Revision History

Rivision	Date	Content	Author	Reviewers
1.0	May 05,25,2019	Initial	Kevin	Jason
1.0	August	Add Uart info	Kevin	Jason

Content

1 Introduction

DB-N8MM is a development board developed by NXP i.MX8MMini SoC as the main control system. It is a small development board with specific functions. It is composed of upper die system and carrier plate.

1.1 Supporting Products

- SoM-N8MM
- Gum Stick
- CBD96-N8MM
- DB-N8MM

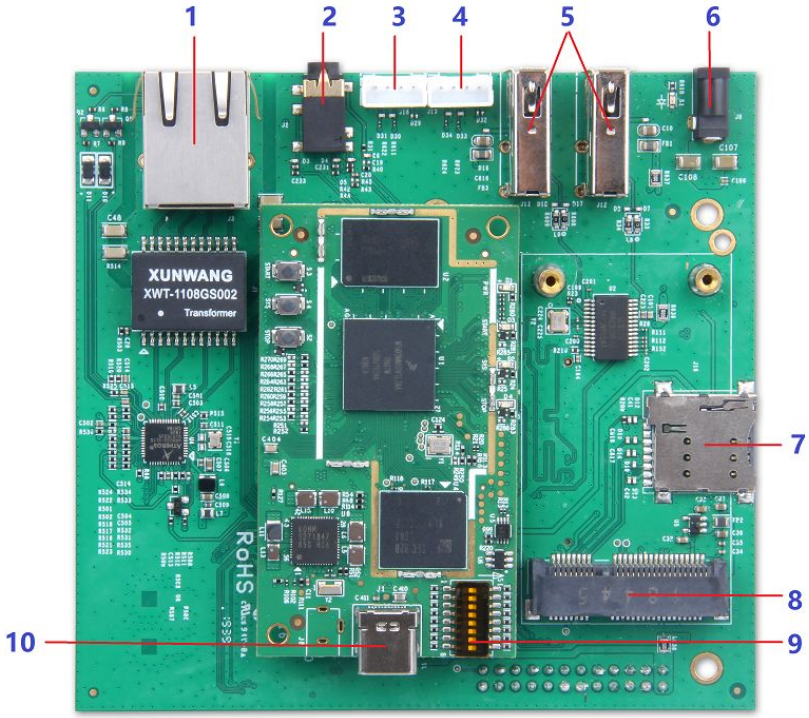
1.2 Key features

Type	Description
Multicore Processing	4x Cortex-A53 core platforms up to 1.8GHz per core 32KB L1-I Cache/ 32 kB L1-D Cache 512 kB L2 Cache 1x Cortex-M4 core up to 400MHz 16 kB L1-I Cache/ 16 kB L2-D Cache
GPU	3D GPU (1x shader, OpenGL® ES 2.0) 2D GPU
Memory/Storage	1GB~4GB LPDDR4 1866MHz 8GB~32GB eMMC5.1 SD 3.0 (UHS-I)
Video Playback	1080p60 VP9 Profile 0, 2 (10-bit) decoder, HEVC/H.265 decoder, AVC/H.264 Baseline, Main, High decoder, VP8 decoder 1080p60 AVC/H.264 encoder, VP8 encoder
Audio	5x SAI (12Tx + 16Rx external I2S lanes), 8ch PDM input
Camero Interface	1x MIPI CSI (4-lane) with PHY
Connectivity	Dual band Wi-Fi 5 2×2MIMO Bluetooth 4.1 On-board BT and WLAN antenna
Peripheral	USB*2 Key*3 TF slot*1 SIM slot*1 DIP switch*1 Type C*1(usb 2.0 only) Audio*1 Ethernet*1 PCIe*1 LoRa*2

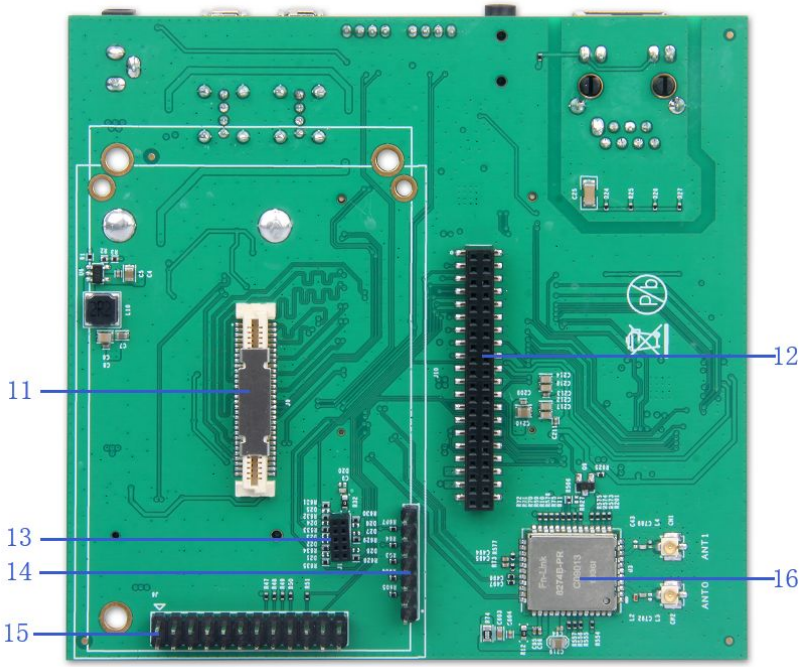
Indicator	User controllable • 3 KEY indicators • 4 LED indicators
OS-support	Linux(Yocto) Android
Expansion connector	• 2x 80 pin High-Speed connector Uart*4,IIC*4,MIPI DSI*1,MIPI CSI*1,PCIe*1,SPI*2,USB*1,GPIO*18 SAI*2,Eth*1,Audio*1 • 1x40 pin Mezznine boards High-Speed connector MIPI CSI*1,MIPI DSI*1,USB*1,IIC*2 • 1x20 pin Mezznine boards Low-Speed connector Uart*2,IIC*1,GPIO*13,SPI*1 • GT-IoT connectpr Uart *1, SPI*1,GPIO*2,Power(3.3V)*1
Size (mm)	CoreBoard:70 x 40 CarryBoard:
Operating Temperature	0°C to +70°C(Standard) -40°C to +85°C(optional)
Net Weight (g)	CoreBoard:15
Power	DC5V

Table 1

2 What's in the board



Top View



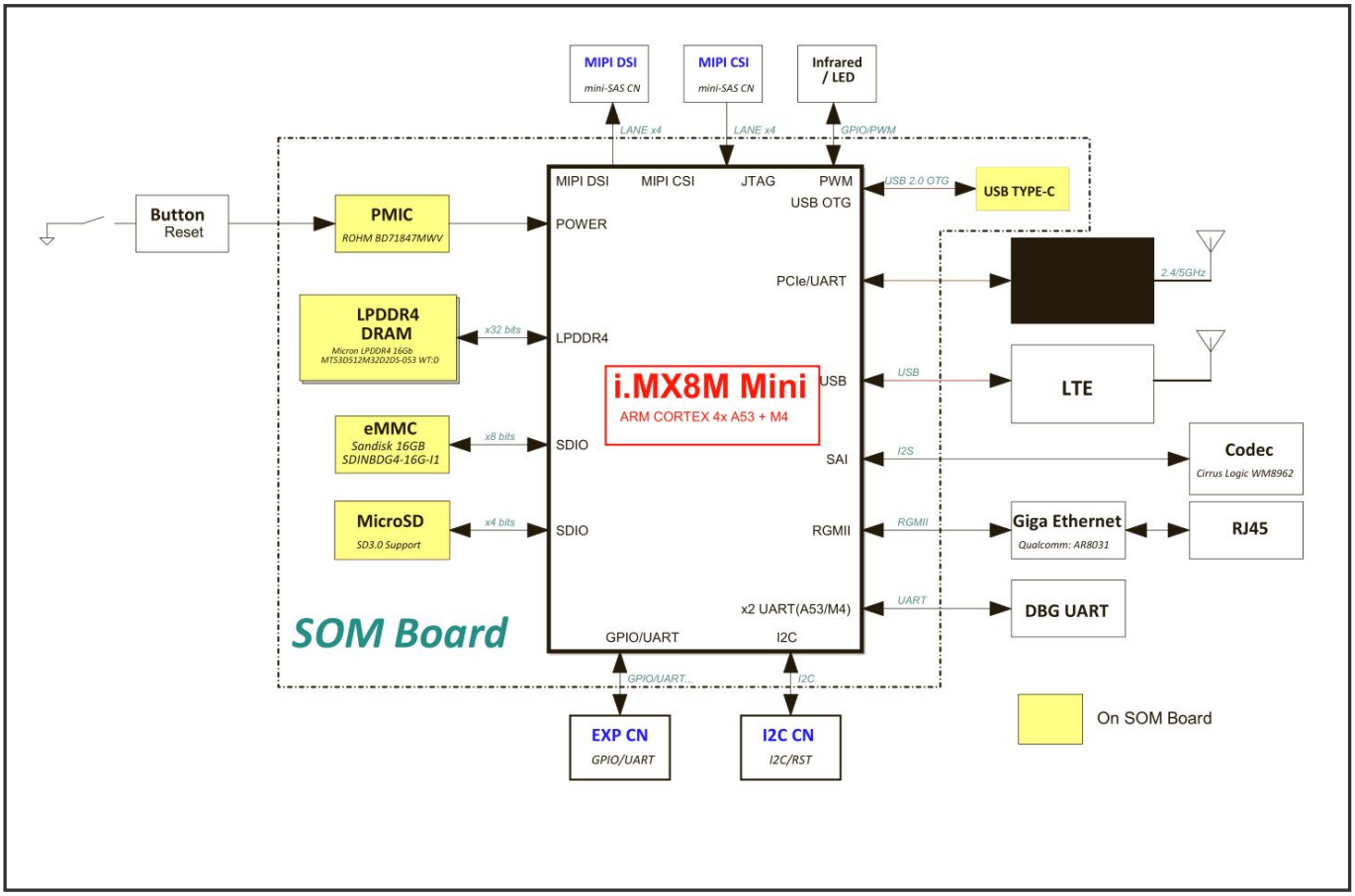
Bottom View

No.	Function	No.	Function	No.	Function	No.	Function
1(J3)	Gigabit Ethernet	5(J13&J12)	USB2.0 Type A - HOST	9(S1)	BOOT switch	13(J11)	GT-IoT Interface
2(J2)	LINE OUT and MIC IN	6(J8)	DC: 5V	10(J1)	USB2.0 (Type C)	14(J7)	SPI Interface1（for LoRa）
3(J18)	UART For A53 Debug	7(J16)	SIM Card Slot	11(J9)	High speed expansion connector	15(J6)	SPI Interface2（for LoRa）
4(J19)	UART For M4 Debug	8(J17)	Mini-PCIe	12(J10)	Low speed expansion connector	16(U3)	RF WiFI/BLE module

Table 2 An overview of the interface

3 Function Overview

3.1 System Block diagram



3.2 Processor

The i.MX8MMini applications processor represents NXP's latest video and audio experience combining state-of-the-art media-specific features with high-performance processing while optimized for lowest power consumption. The i.MX 8M Mini family of processors features advanced implementation of a quad Arm® Cortex®-A53 core, which operates at speeds of up to 1.6 GHz. A general purpose Cortex®-M4 400 MHz core processor is for low-power processing. The DRAM controller supports 32-bit/16-bit LPDDR4, DDR4, and DDR3L memory. A wide range of audio interfaces are available, including I2S, AC97, TDM, and S/PDIF. There are a number of other interfaces for connecting peripherals, such as USB, PCIe, and Ethernet.

Video Processing Unit:

- **1080p60 VP9 Profile 0, 2 (10-bit)**
- **1080p60 HEVC/H.265 Decoder**
- **1080p60 AVC/H.264 Baseline, Main, High decoder**
- **1080p60 VP8**
- **1080p60 AVC/H.264 Encoder**
- **1080p60 VP8**
- **TrustZone support**

3.3 Memory

This design USES SDRAM-mobile - LPDDR4-memory - IC-16GB (512m-x-32) - 1866MHZ-200-WFBGA

(10x14.5), with 2GB memory, low power consumption characteristics.

Key Feature：

- Ultra-low-voltage core and I/O power supplies
  - VDD1 = 1.70 – 1.95V; 1.80V nominal
  - VDD2 = 1.06 – 1.17V; 1.10V nominal
  - VDDQ = 1.06 – 1.17V; 1.10V nominal or Low VDDQ = 0.57 – 0.65V; 0.60V nominal
- Frequency range
  - 2133 – 10 MHz (data rate range: 4266 – 20 Mb/s/ pin)
- 16n prefetch DDR architecture
- 8 internal banks per channel for concurrent operation
- Single-data-rate CMD/ADR entry
- Bidirectional/differential data strobe per byte lane
- Programmable READ and WRITE latencies (RL/WL)
- Programmable and on-the-fly burst lengths (BL = 16, 32)
- Directed per-bank refresh for concurrent bank operation and ease of command scheduling
- Up to 8.5 GB/s per die
- On-chip temperature sensor to control self refresh rate
- Partial-array self refresh (PASR)
- Selectable output drive strength (DS)
- Clock-stop capability
- RoHS-compliant, “green” packaging
- Programmable VSS (ODT) termination
- AEC-Q100

3.4 Micro-SDHC

The SoM-N8MM(GumStick) Micro-SD slot (J7) signals are routed directly to the i.MX8M Mini SDC2 interface. The slot is a push-push type with a dedicated support for card detect signal (many Micro-SD slots do not have a dedicated CD pins, they use DATA3 state as the card detected signal). The DB4 uses GPIO1_IO15 as the SD_CARD_DET.

3.5 Ethernet

The AR8033 Ethernet transceiver is a single port, 10/100/1000 Mbps tri-speed Ethernet PHY. The AR8033 Ethernet transceiver supports both RGMII and SGMII to the MAC. The AR8033 Ethernet transceiver belongs to the Arctic™ PHY family which provides a low power, low BOM cost solution for comprehensive applications including enterprise, carrier and home networks such as CPE, home gateway, enterprise switch, carrier switch/router, mobile base station and base station controller, optical module and media converter, industrial automation and measurement.

3.6 WiFi/BT(BLE)

The design uses the Fn-link8274B-PR Module, which is a PCIe interface communication, dual channel, Highly integrated wireless local area network (WLAN) system-on-chip (SOC) for 5 GHZ 802.11ac, or 2.4G /5G 802.11n WLAN applications.

Key Feature：

- Dual-stream spatial multiplexing up to 867 Mbps data rate
- Supports BLE5.0
- Supports 20/40MHz at 2.4GHz and supports 20/40/80MHz at 5GHz
- Supports low power PCI-e interface for WLAN and UART/PCM interface for Bluetooth.
- Supports Bluetooth V4.2+HS, BLE and be backwards compatible with Bluetooth 1.2, 2.X+ enhance data rate.
- Supports WLAN-Bluetooth coexistence and ISM-LTE coexistence.
- Supports Bluetooth for class1 and class2 power level transmissions without requiring an external PA.
- BT host digital interface:
  - HCI UART (up to 4 Mbps)
  - PCM for audio data

3.7 MIPI

- **4-lane MIPI-DSI Interface**
- **4-lane MIPI-CSI Interface**

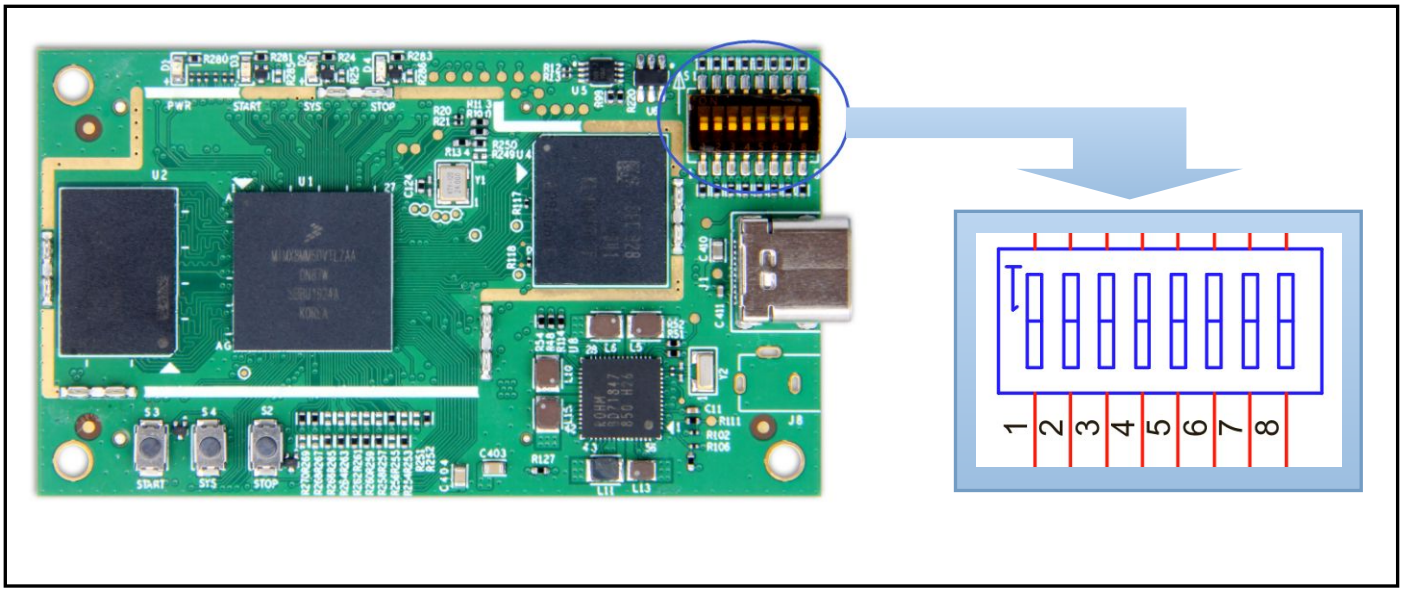
3.7.1 MIPI DSI

This module provides a four-lane MIPI display serial interface operating up to a maximum bit rate of 1.5 Gbps. Support up to 1080p60 display through MIPI DSI.

3.7.2 MIPI CSI

This module provides one four-lane MIPI camera serial interfaces,which operates up to a maximum bit rate of 1.5 Gbps

3.8 BOOT switch



3.81 BOOT Settings

Boot Device	Boot Mode		Internal Boot (SW1 [3-8])					
eMMC/SDHC3	BOOT_MODE 1	BOOT_MODE 0	1	0	1	0	1	0
MicroSD/SDHC2			0	1	0	1	0	1

Table 2

BOOT TYPE:

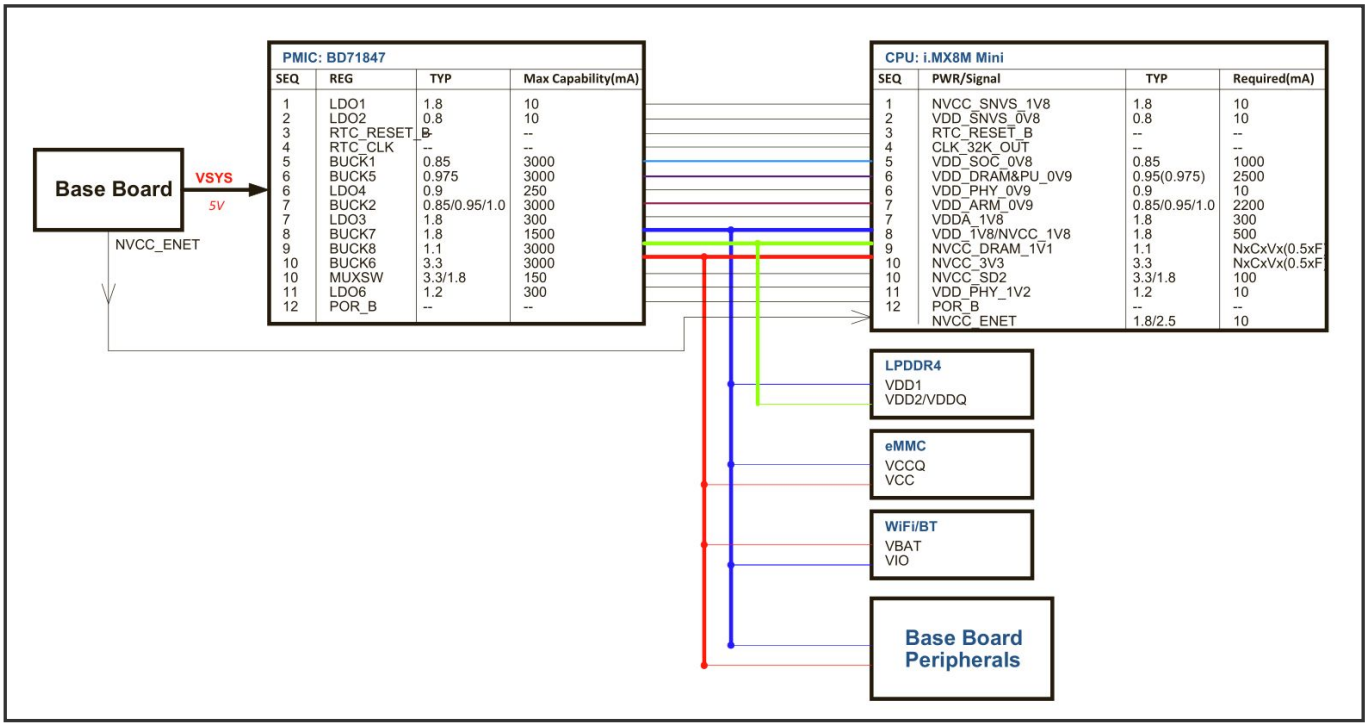
00 Boot From Fuses

01 Serial Downloader

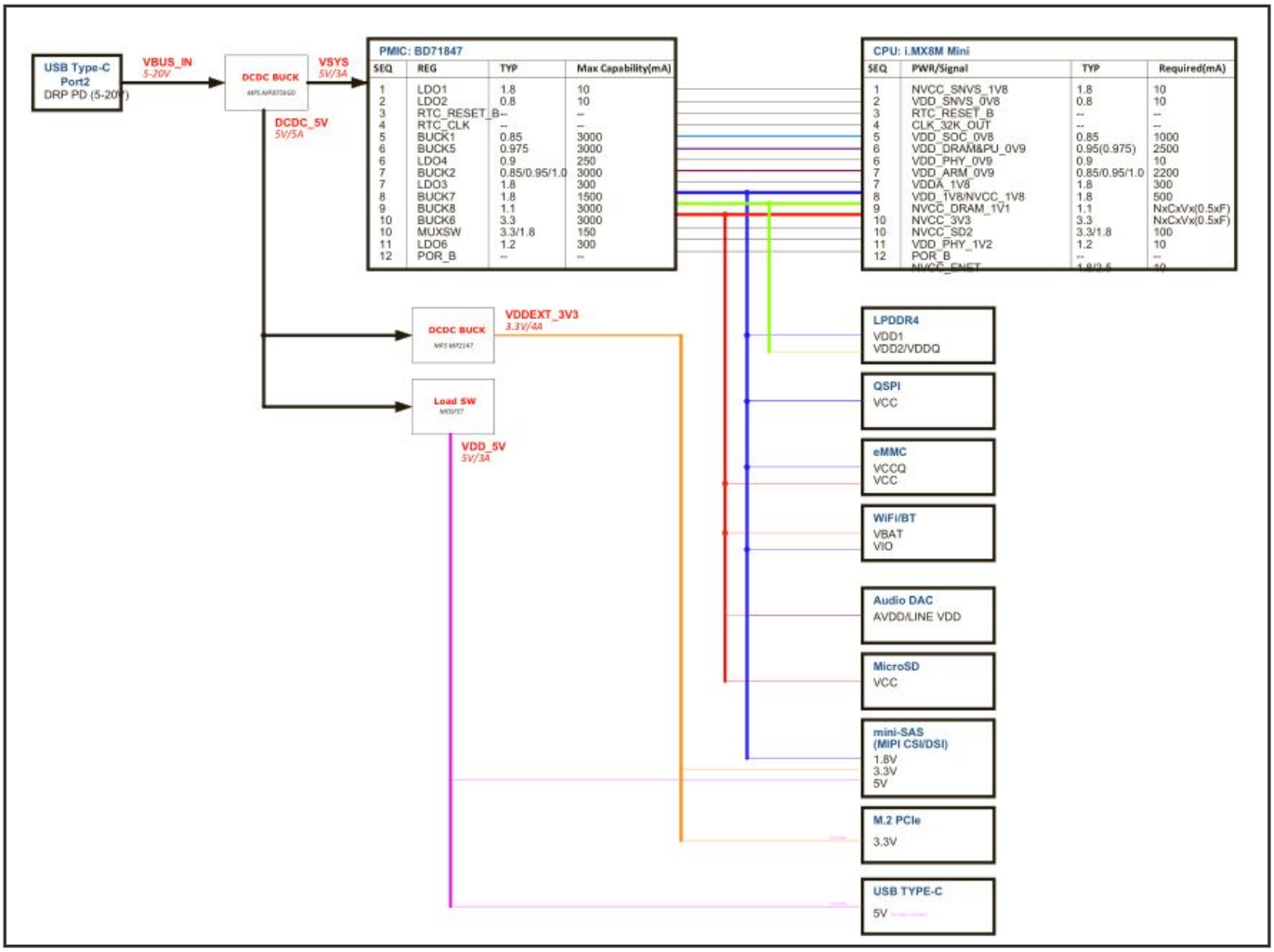
10 Internal Boot (Development)

11 Reserved

3.9 Power Block diagram(Main Board)

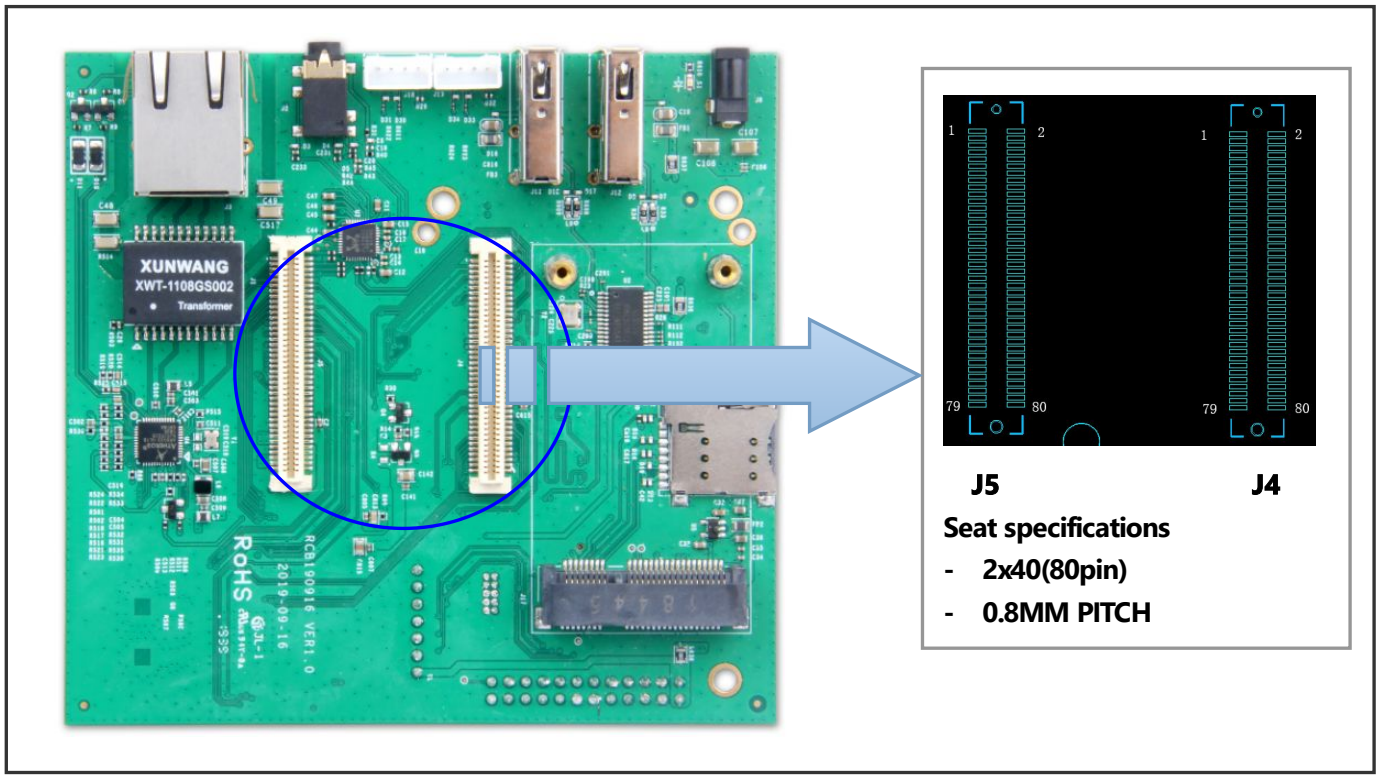


3.10 Power Block diagram(Carry Board)



4 High speed expansion connector(2x80)

4.1 Position and specification



4.2 80PIN high speed Connector (J5)

Pin No.	Pin definition	I/O Properties	Pin No.	Pin definition	I/O Properties
1	GND		2	GND	
3	UART3_RTS	Input	4	ECSPI2_SS0	output
5	UART3_RXD	Input	6	ECSPI2_SCLK	output
7	UART3_TXD	Input	8	ECSPI2_MISO	Input
9	UART3_CTS	Input	10	ECSPI2_MOSI	output
11	GND		12	GND	
13	I2C3_SCL	Input	14	I2C_SCL2	Output low
15	I2C3_SDA	Input	16	I2C_SDA2	Output low
17	I2C4_SCL	Input	18	GND	
19	I2C4_SDA	Input	20	DSI_DN0	Output low
21	GND		22	DSI_DP0	Output low
23	DSI_DN1	Output low	24	GND	
25	DSI_DP1	Output low	26	DSI_CKN	Input

27	GND		28	DSI_CKP	Output low
29	DSI_DN2	Output low	30	GND	
31	DSI_DP2	Output low	32	DSI_DN3	Output low
33	GND		34	DSI_DP3	Output low
35	CSI_DN0	Output low	36	GND	
37	CSI_DP0	Output low	38	CSI_DN1	Output low
39	GND		40	CSI_DP1	Output low
41	CSI_CKN	Output low	42	GND	
43	CSI_CKP	Output low	44	CSI_DN2	Output low
45	GND		46	CSI_DP2	Output low
47	CSI_DN3	Output low	48	GND	
49	CSI_DP3	Output low	50	PCIE_RXN	Output low
51	GND		52	PCIE_RXP	Output low
53	PCIE_TXN		54	GND	
55	PCIE_TXP		56	PCIE_CLKN	Output low
57	GND		58	PCIE_CLKP	Output low
59	BT_TXD		60	GND	
61	BT_RXD		62	USB2_DN	
63	BT_RTS		64	USB2_DP	
65	BT_CTS		66	GND	
67	GND		68	GPIO3_IO00 6	Input/output
69	UART2_TXD 13	Input	70	GPIO3_IO01 6	Input/output
71	UART2_RXD 13	Input	72	GPIO2_IO17	Input/output
73	UART4_TXD 13	Input	74	GPIO2_IO18	Input/output
75	UART4_RXD	Input	76	GPIO2_IO11	Input/output
77	GND		78	GND	
79	PCIe_nWAKE		80	TCPC_nINT2	

Table 3

4.3 80PIN high speed Connector (J4)

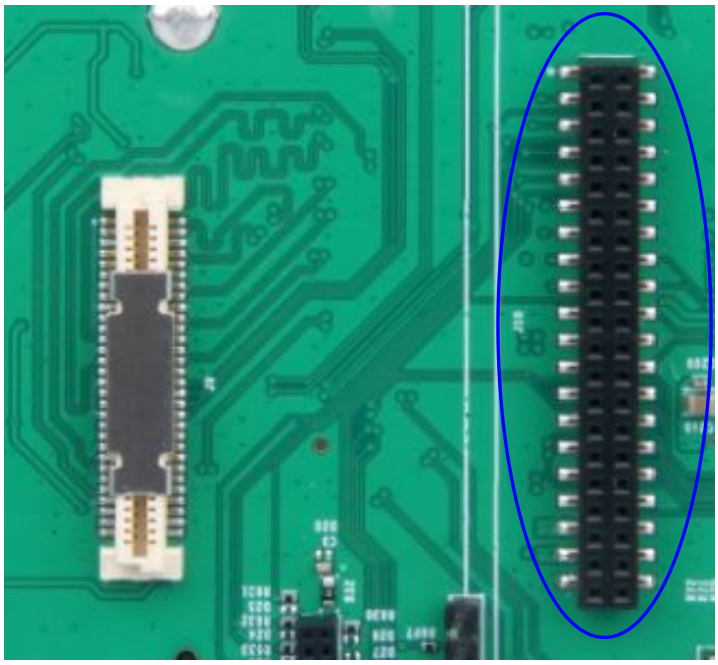
Pin No.	Pin definition	I/O Properties	Pin No.	Pin definition	I/O Properties
1	SAI3_MCLK		2	IR_CAP 6	
3	SAI3_TXFS		4	GPIO1_IO12 6	Input/output
5	SAI3_TXC		6	ENET_WoL 6	
7	GND		8	ENET_nINT 6	
9	SAI3_TXD		10	DSI_TS_nINT 6	
11	SAI3_RXFS		12	DSI_EN	
13	SAI3_RXC		14	GND	
15	SAI3_RXD		16	CSI_PWDN 6	
17	GND		18	CSI_nRST 6	
19	REF_CLK_32K		20	PCIe_nDIS_LV 6	
21	BT_WAKE_HOST		22	DSI_BL_PWM 6	
23	BT_WAKE_DEV		24	PCIe_nRST_LV 6	
25	WL_WAKE_HOST		26	ENET_nRST_LV 6	
27	WL_REG_ON		28	GND	
29	BT_REG_ON		30	ENET_RX_CTL 6	
31	GND		32	GND	
33	SAI2_TXC		34	ENET_RXC 6	
35	SAI2_TXFS		36	GND	
37	SAI2_TXD		38	ENET_RD0	
39	SAI2_RXD		40	ENET_RD1	
41	GND		42	ENET_RD2	
43	ENET_TX_CTL		44	ENET_RD3	
45	GND		46	GND	
47	ENET_TXC		48	ENET_MDC	
49	GND		50	ENET_MDIO	
51	ENET_TD0		52	GND	
53	ENET_TD1		54	GPIO2_IO00	Input/output
55	ENET_TD2		56	GPIO2_IO01	Input/output

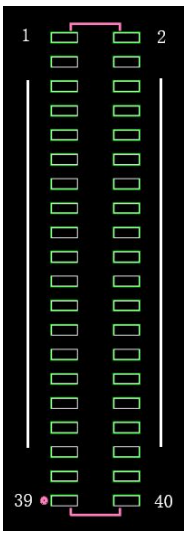
57	ENET_TD3		58	GPIO2_IO15	Input/output
59	GND		60	GPIO2_IO16	Input/output
61	NVCC_ENET		62	GND	
63	GND		64	GND	
65	GND		66	GND	
67	GND		68	VDD_1V8	
69	GND		70	VDD_1V8	
71	VSYS_5V		72	GND	
73	VSYS_5V		74	GND	
75	VSYS_5V		76	VDD_3V3	
77	VSYS_5V	Power input	78	VDD_3V3	
79	VSYS_5V		80	GND	

Table 4

5 Low speed Expansion connector(2x20)

5.1 Position and specification





J10

Seat specifications

- **2x20(40pin)**
- **2.0MM PITCH**

5.2 40PIN high speed Connector (J10)

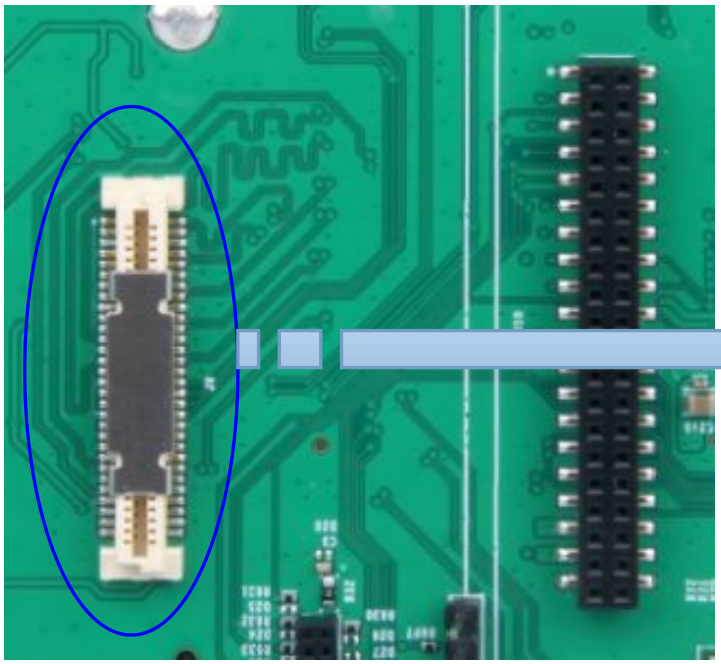
Pin No.	96Boards pin definition	DB-iMX8M Mini Series pin definition	Pin No.	96Boards pin definition	DB-iMX8M Mini Series pin definition
1	GND	GND	2	GND	GND
3	UART0_CTS	UART3_CTS	4	PWR_BTN_N	N.C.
5	UART0_TxD	UART3_TXD	6	RST_BTN_N	N.C.
7	UART0_RxD	UART3_RXD	8	SPI0_SCLK	SPI0_CLK (APQ GPIO_19)
9	UART0_RTS	UART3_RTS	10	SPI0_DIN	SPI0_MISO (APQ GPIO_17)
11	UART1_TxD	UART2_TXD	12	SPI0_CS	SPI0_CS_N (APQ GPIO_18)
13	UART1_RxD	UART2_RXD	14	SPI0_DOUT	SPI0_MOSI (APQ GPIO_16)
15	I2C0_SCL	I2C4_SCL	16	PCM_FS	GPIO2_IO00
17	I2C0_SDA	I2C4_SDA	18	PCM_CLK	GPIO2_IO01
19	I2C1_SCL	N.C.	20	PCM_DO	GPIO2_IO02
21	I2C1_SDA	N.C.	22	PCM_DI	N.C.
23	GPIO-A	GPIO1_IO01	24	GPIO-B	GPIO2_IO03
25	GPIO-C	GPIO1_IO05	26	GPIO-D	GPIO2_IO11

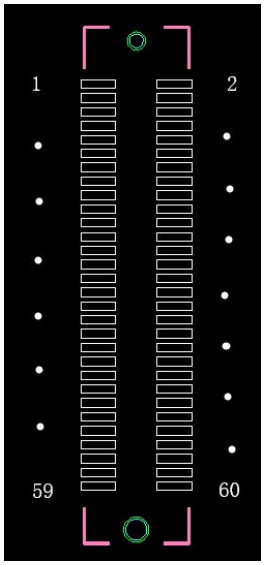
27	GPIO-E	GPIO1_IO08 GPIO2_IO12	28	GPIO-F	GPIO2_IO12
29	GPIO-G	GPIO1_IO09 GPIO4_IO28	30	GPIO-H	GPIO2_IO28
31	GPIO-I	CSI_nRST CSI_PWDN	32	GPIO-J	CSI_PWDN
33	GPIO-K	GPIO1_IO12	34	GPIO-L	GPIO4_IO29
35	+1V8	LS_EXP_1P8(VDD_1V8)	36	SYS_DCIN	N.C.
37	+5V	VDD_5V	38	SYC_DCIN	N.C.
39	GND	GND	40	GND	GND

Table 5

6 High speed expansion connector(2x30Pin)

6.1 Position and specification





J9

Seat specifications

- **2x30(60pin)**
- **0.8MM PITCH**

6.2 60PIN high speed Connector (J9)

Pin No.	96Boards CE pin definition	DB-iMX8M Mini Series pin definition	Pin No.	96Boards CE pin definition	DB-iMX8M Mini Series pin definition
1	SD_DAT0/SPI1_DOUT	SPI1_MOSI (APQ GPIO_8)	2	CSI0_C+	CSI_CKP
3	SD_DAT1	N.C.	4	CSI0_C-	CSI_CKN
5	SD_DAT2	N.C.	6	GND	GND
7	SD_DAT3/SPI1_CS	N.C.	8	CSI0_D0+	CSI_DP0
9	SD_SCLK/SPI1_SCLK	N.C.	10	CSI0_D0-	CSI_DN0
11	SD_CMD/SPI1_DIN	N.C.	12	GND	GND
13	GND	GND	14	CSI0_D1+	CSI_DP1
15	CLK0/CSI0_MCLK	N.C.	16	CCSI0_D1-	CSI_DN1
17	CLK1/CSI1_MCLK	N.C.	18	GND	GND
19	GND	GND	20	CSI0_D2+	CSI_DP2

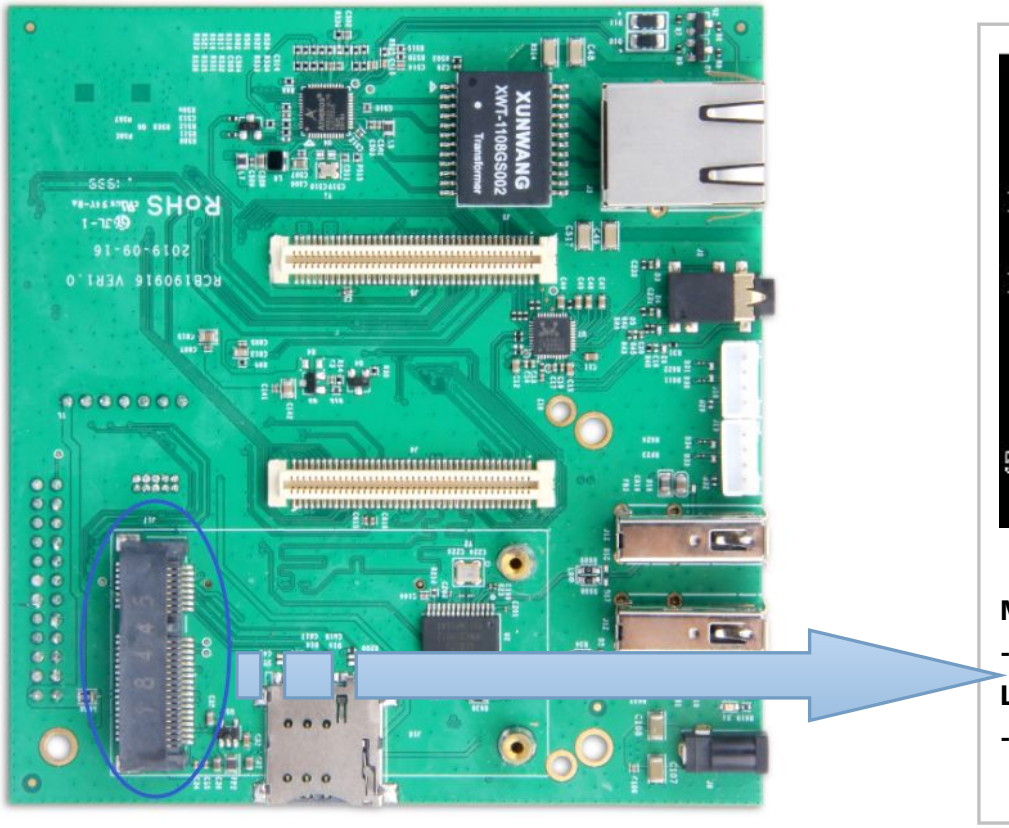
21	DSI_CLK+	DSI_CKP	22	CSI0_D2-	CSI_DN2
23	DSI_CLK-	DSI_CKN	24	GND	GND
25	GND	GND	26	CSI0_D3+	CSI_DP3
27	DSI_D0+	DSI_DP0	28	CSI0_D3	CSI_DN3
29	DSI_D0-	DSI_DN0	30	GND	GND
31	GND	GND	32	I2C2_SCL	I2C2_SCL_3V3
33	DSI_D1+	DSI_DP1	34	I2C2_SCL	I2C2_SDA_3V3
35	DSI_D1-	DSI_DN1	36	I2C3_SDA	I2C3_SCL
37	GND	GND	38	I2C3_SDA	I2C3_SDA
39	DSI_D2+	DSI_DP2	40	GND	GND
41	DSI_D2-	DSI_DN2	42	CSI1_D0+	N.C.
43	GND	GND	44	CSI1_D0-	N.C.
45	DSI_D3+	DSI_DP3	46	GND	GND
47	DSI_D3-	DSI_DN3	48	CSI1_D1+	N.C.
49	GND	GND	50	CSI1_D1-	N.C.
51	USB_D+	USB_EXP_P	52	GND	GND
53	USB_D-	USB_EXP_N	54	CSI1_C+	N.C.
55	GND	GND	56	CSI1_C-	N.C.
57	HSIC_STR	N.C.	58	GND	GND
59	HSIC_DATA	N.C.	60	RESERVED	N.C.

Table 6 HS(96Board CE) pin definition

7 Mini-PCIe Interface

This design PCIE interface (USB bus) is designed for LTE module (please contact Geniatech for confirmation if you want to know the specific model). This product supports LTE modules such as Chinese regulation, Japanese regulation, European regulation, American regulation and Australian regulation.

7.1 Position and specification



7.2 Mini-PCIe pin definition

Pin No.	MiniPCIe standard pin definition	DB-iMX8M Mini Series pin definition	I/O Properties	Description
1	WAKE#	NC	Analog input	Analog audio input positive
2	3.3Vaux	PCIe_3.3V	Power input	3.3 V power supply
3	COEX1	NC	Analog input	Analog audio input negative
4	GND	GND		Ground
5	COEX2	NC	Analog output	Analog audio output positive
6	1.5V	PCIe_1.5V		No use
7	CLKREQ#	Test Point	Analog output	Analog audio output negative
8	UIM_PWR	PCIE_UIM_PWR	Power output	USIM Card Power supply

9	GND	GND		Ground
10	UIM_DATA	PCIE_UIM_DATA	Input/output	USIM card data
11	REFCLK-	NC	Input	PCI-e Differential Reference clock negative(100 MHz)
12	UIM_CLK	PCIE_UIM_CLK	Output	USIM Card Clock
13	REFCLK+	NC	Output	PCI-e Differential Reference clock positive(100 MHz)
14	UIM_RESET	PCIE_UIM_RST	Output	USIM Card reset
15	GND	GND		Ground
16	UIM_Vpp	PCIE_UIM_VPP		USIM Card Programmable voltage
17	Reserved	NC	Output	No use
18	GND	GND		Ground
19	Reserved	NC	Input/output	No use
20	W_DISABLE#	Test Point	Input	Rf ban control, "low" effective
21	GND	GND		Ground
22	PERST#	Test Point	Input	Reset control, "low" effective
23	PERn0	NC	Input	Differential receive pair negative
24	3.3Vaux	PCIe_3.3V	Power input	3.3 V power supply
25	PERp0	NC	Output	Differential receive pair positive
26	GND	GND		Ground
27	GND	GND		Ground
28	1.5V	NC		No use
29	GND	GND		Ground
30	SMB_CLK	NC	Output	USMBus clock signal compliant to the SMBUS2.0 specification
31	PETn0	NC	Input	Differential transmit pair -
32	SMB_DATA	NC	Input/output	USMBus data signal compliant to the SMBUS2.0 specification
33	PETp0	NC	Output	Differential transmit pair +
34	GND	GND		Ground
35	GND	GND		Ground
36	USB_D-	USB_HOST3_DN	Input/output	USB data-
37	GND	GND		Ground

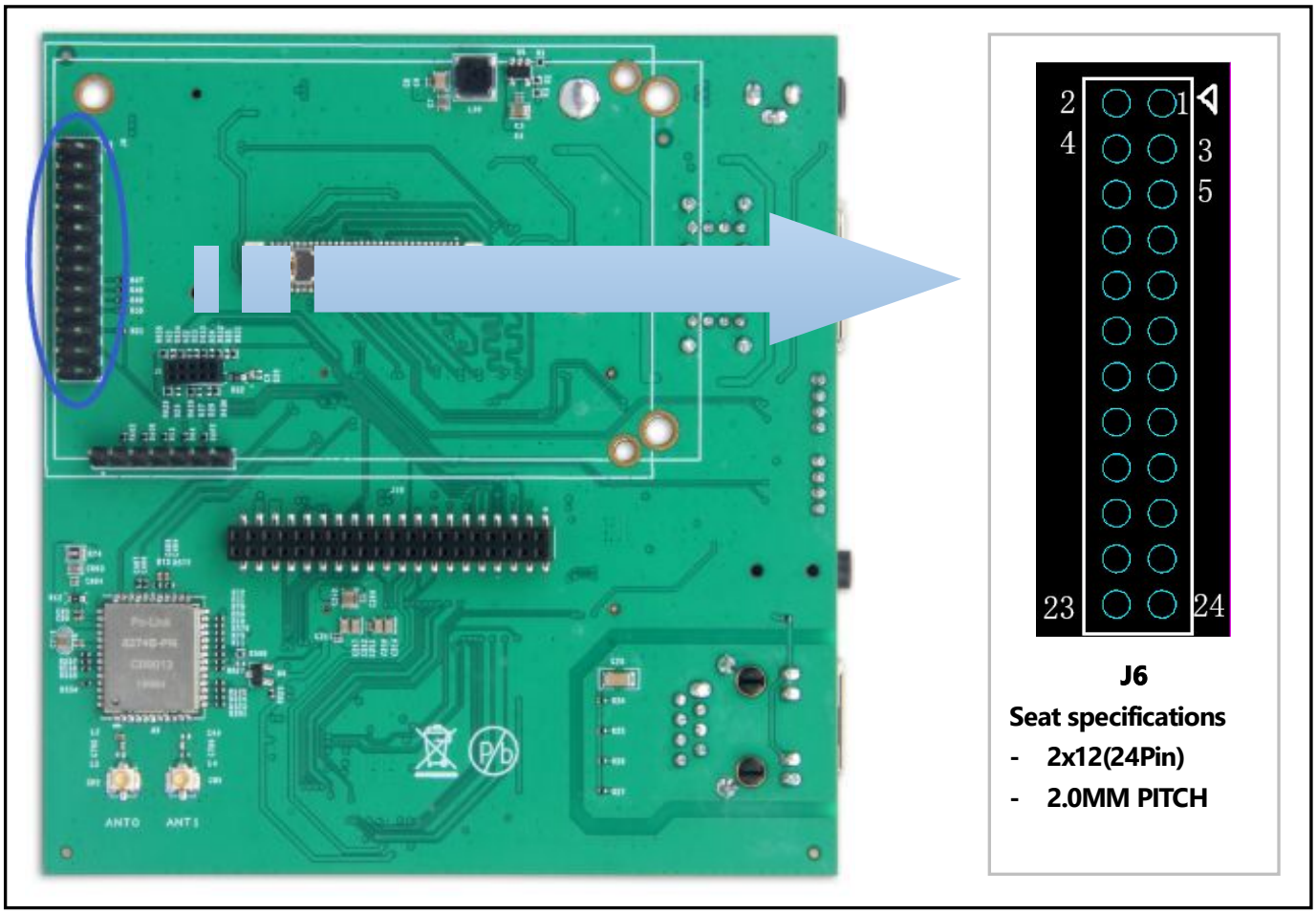
38	USB_D+	USB_HOST3_DP	Input/output	USB data+
39	3.3Vaux	PCIe_3.3V	Power input	3.3 V power supply
40	GND	GND		Ground
41	3.3Vaux	PCIe_3.3V	Power input	3.3 V power supply
42	LED_WWAN#	NC	Current input	Active low signals
43	GND	GND		Ground
44	LED_WLAN#	NC	Input	Active low signals
45	Reserved	NC	Input/output	No use
46	LED_WPAN#	NC	Output	Active low signals
47	Reserved	NC	Input/output	No use
48	1.5V	NC		No use
49	Reserved	NC	Input/output	No use
50	GND	GND		Ground
51	Reserved	NC	Input/output	No use
52	3.3Vaux	PCIe_3.3V	Power input	3.3 V power supply

Table 7

8 IoT connector(2x12 Pin)_LoRa Modul 1

This design interface (SPI bus) is designed for LoRa module (please contact Geniatech for details), and of course supports other modules that meet the DEFINITION of SPI.

8.1 Position and specification



8.2 2*24Pin definition

Pin No.	Geniatech all Series pin definition	I/O Properties	Description
1	VCC_5V		
2	VCC_5V		
3	GND		
4	N.C.		
5	GND		
6	GND		
7	SPI_MISO	Input with PD	
8	N.C.		

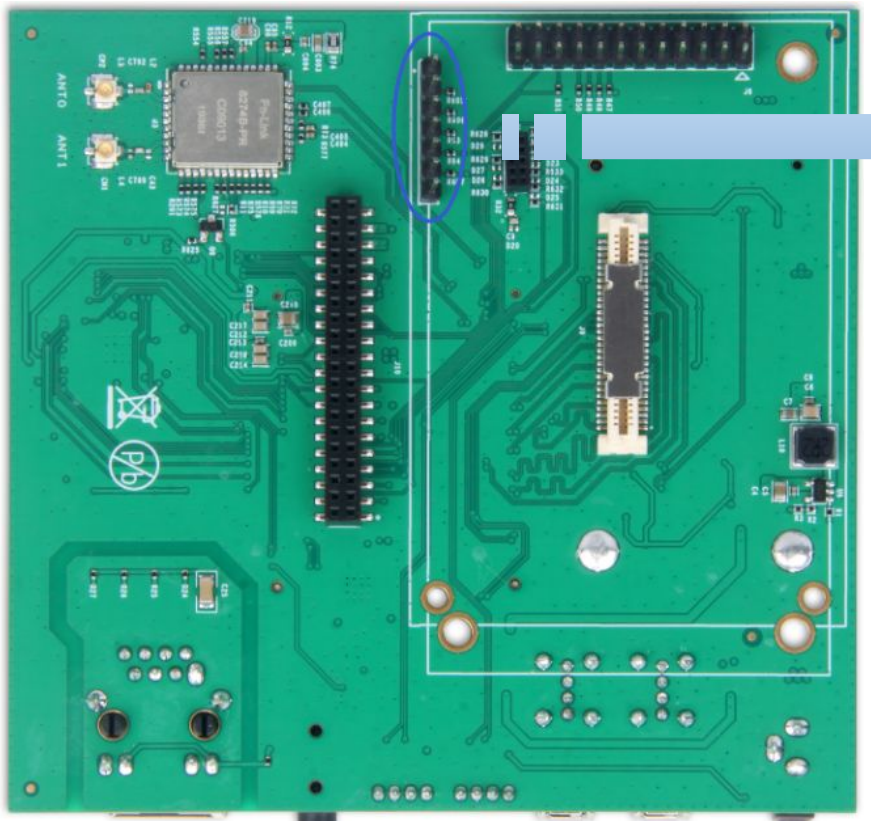
9	N.C.		
10	GPIO	GPIO2_IO05	
12	GND		
13	N.C.		
14	GND		
15	SPI_CS_2	Input with PD	
16	SPI_MOSI_2	Input with PD	
17	N.C.		
18	SPI_CLKI_2	Input with PD	
19	LoRa_RESET		
20	N.C.		
21	LoRa_state		
22	N.C.		
23	N.C.		
24	N.C.		

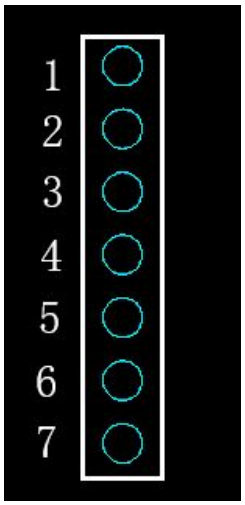
Table 8

9 LoRa connector (7Pin)_LoRa Modul 2

This design interface (SPI bus) is designed for LoRa module (please contact Geniatech for details), and of course supports other modules that meet the DEFINITION of SPI.

9.1 Position and specification





J7

Seat specifications

- **1x7(7Pin)**
- **2.0MM PITCH**

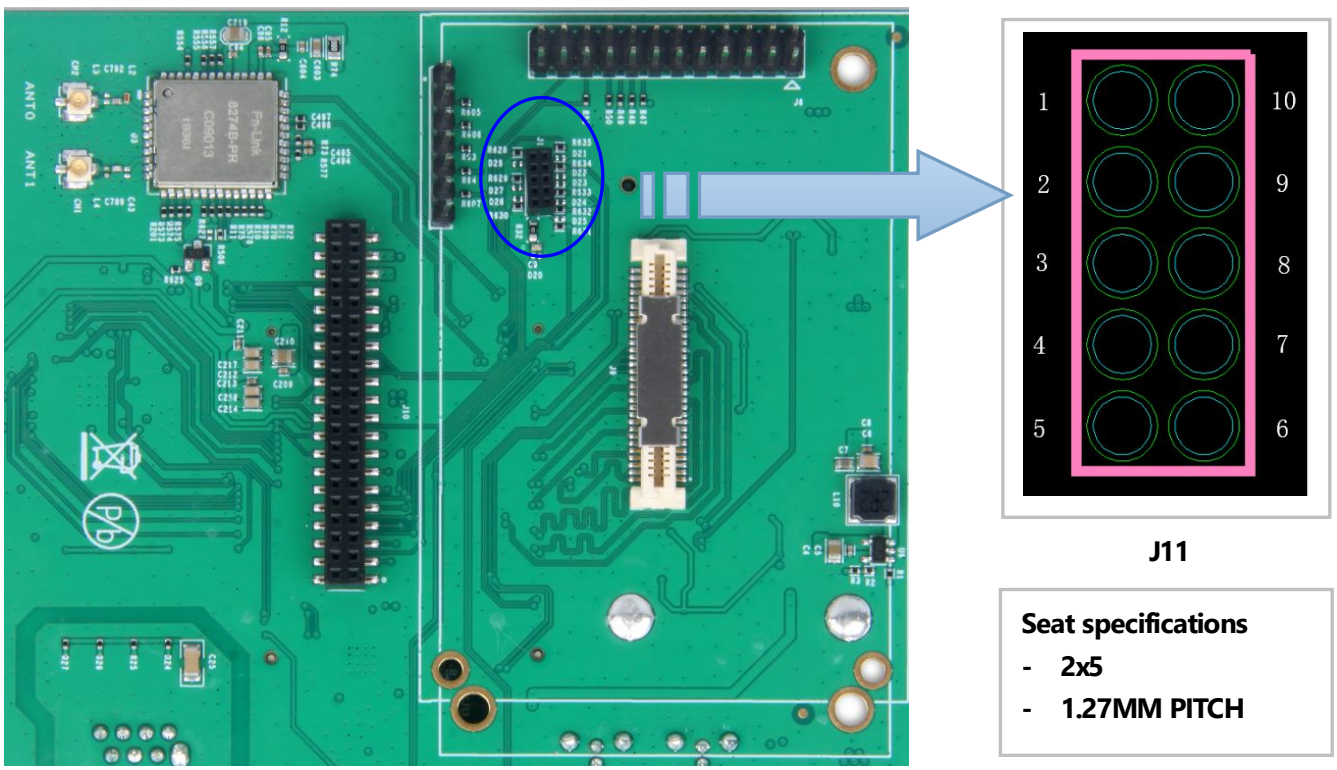
9.2 7Pin definition

Pin No.	Geniatech all Series pin definition	I/O Properties	Description
1	VCC_5V	GPIO2_IO09	
2	SPI_CS_2	Input with PD	
3	SPI_CLKI_2	Input with PD	
4	SPI_MISO	Input with PD	
5	SPI_MOSI_2	Input with PD	
6	LoRa_RESET	/	
7	GND		

Table 9

10 GT-IoT Interface

Gt-iot is Geniatech's universal physical interface for Internet of Things devices. It defines A UART and SPI bus that can be connected to BLE, ZigBee, Z-Wave and other extension modules.



10.1 10Pin definition

Pin No.	Geniatech all Series pin definition	I/O Properties	Description
1	GPIO/RST	GPIO2_IO09	
2	GND	/	
3	UART TX	Input with PD	
4	UART RX	Input with PD	
5	VCC	Power input	
6	SPI_MOSI	Input with PD	
7	SPI_MISO	Input with PD	
8	SPI_CS	Input with PD	
9	SPI_CLK	Input with PD	
10	GPIO	GPIO2_IO05	

Table 10

11 Programmable function

11.1 Programmable function 1: Button

Name	Chip pins	Effective level	programmable
START	NAND_DATA02（CPU Pin K23）	High	Yes
SYS	SYS_nRST（Connect PMU power pin, low level effective）	High	No
STOP	NAND_DATA03（CPU Pin N23）	High	Yes

Table 11

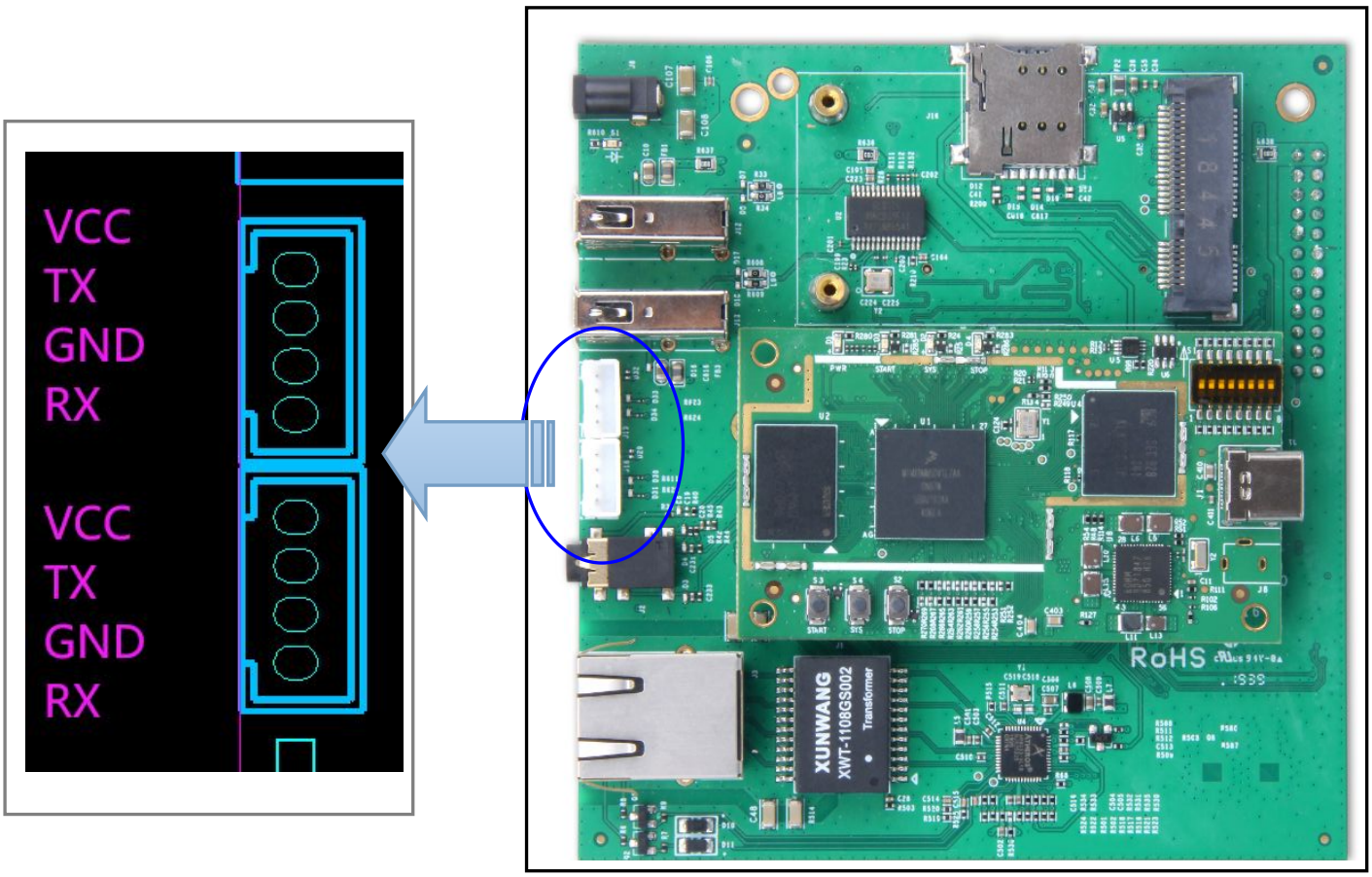
11.2 Programmable function 2: LED

Name	Chip pins	Effective level	Programmable
PWR	Connect 3.3 V	/	No
START	NAND_DATA00(CPU Pin P23)	High	Yes
SYS	NAND_READY_B(CPU Pin P26)	High	Yes
STOP	NAND_DATA01(CPU Pin K24)	High	Yes

Table 12

12 Uart Debug

12.1 Position



12.2 Description

- UART For A53 Debug ((J18)
- UART For M4 Debug (J19)
- Baud rate:115200bps
- Stop bit::1
- Data bits:8
- Parity bit::none

12 Mechanical specification

12.1 Board dimensions